CLAIMS

1. A method of operating a memory device, comprising:

receiving a first subset of a set of command and address signals substantially simultaneous with receiving a first edge of a clock signal;

receiving a second subset of the set of command and address signals substantially simultaneous with receiving a second edge of the clock signal; and

performing a memory command in response to the set of command and address signals.

2. The method of claim 1, wherein the memory device comprises a device selected from the group consisting of a DRAM device, a flash memory device, a volatile memory device, a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device.

3. The method of claim 1, further comprising:

sending the first subset of the set of command and address signals substantially simultaneous with sending the first edge of the clock signal by an external controller; and

sending the second subset of the set of command and address signals substantially simultaneous with sending the second edge of the clock signal by the external controller.

4. The method of claim 3, wherein, in sending, the external controller is a device selected from the group consisting of a DRAM controller, a central processing unit (CPU), a graphics processing unit (GPU), and a processor.

5. A method of operating a memory device, comprising:

receiving a set of command signals and a first subset of a set of address signals substantially simultaneous with receiving a first edge of a clock signal;

receiving a second subset of the set of address signals substantially simultaneous with receiving a second edge of the clock signal; and

performing a memory command in response to the set of command and address signals.

6. The method of claim 5, wherein the memory device comprises a device selected from the group consisting of a DRAM device, a flash memory device, a volatile memory device, a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device.

7. The method of claim 5, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively.

8. A method of operating a memory device, comprising:

receiving a first subset of a set of command and address signals substantially simultaneous with receiving a first edge of a first cycle of a clock signal;

receiving a second subset of the set of command and address signals substantially simultaneous with receiving a first edge of a second cycle of the clock signal; and

performing a memory command in response to the set of command and address signals.

9. The method of claim 8, wherein, in receiving the second subset of command and address signals, the second cycle is substantially subsequent to the first cycle.

10. The method of claim 8, wherein the memory device comprising a device selected from the group consisting of a DRAM device, a flash memory device, a

volatile memory device, a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device.

11. A method of operating a memory device, comprising:

receiving a set of command signals and a first subset of a set of address signals substantially simultaneous with receiving a first edge of a first cycle of a clock signal;

receiving a second subset of the set of address signals substantially simultaneous with receiving a first edge of a second clock cycle of the clock signal; and

performing a memory command in response to the set of command and address signals.

12. The method of claim 11, wherein, in receiving the second subset of the set of address signals, the second cycle is substantially subsequent to the first cycle.

13. The method of claim 11, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively.

14. The method of claim 11 wherein the memory device comprising a device selected from the group consisting of a DRAM device, a flash memory device, a volatile memory device, a non-volatile memory device, a static random access operating memory (SRAM) device, and a static memory device.

15. A memory device comprising:

multiple command and address pins to receive a first subset of a set of command and address signals substantially simultaneous with receiving a first edge

of a clock signal, wherein the multiple command and address pins to further receive a second subset of the set of command and address signals substantially simultaneous with receiving a second edge of a clock signal, and wherein the memory device operates to perform a memory command in response to the set of received command and address signals.

16. The memory device of claim 15, wherein the memory device is a device selected from the group consisting of a DRAM device, a flash memory device, a volatile memory device, a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device.

17. The memory device of claim 15, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively.

18. A memory device comprising:

multiple command and address pins to receive a first subset of a set of command and address signals substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein the multiple command and address pins to further receive a second subset of the set of command and address signals substantially simultaneous with receiving a first edge of a second cycle of the clock signal, and wherein the memory device to perform a memory command in response to the set of received command and address signals.

19. The memory device of claim 18, wherein the memory device is a device selected from the group consisting of a DRAM device, a flash memory device, a volatile memory device, a non-volatile memory device, a static random access memory (SRAM) device, and a static memory device.

20. The memory device of claim 18, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively.

21. A memory circuit comprising:

one or more integrated circuit memory devices operable for communicating with an external controller, wherein each of the integrated circuit memory devices operates to receive a first subset of a set of command and address signals substantially simultaneous with receiving a first edge of a clock signal, wherein each of the integrated memory circuit devices operates to receive a second subset of the set of command and address signals substantially simultaneous with receiving a second edge of a clock signal, and wherein each integrated circuit memory device operates to perform a memory command in response to the set of received associated command and address signals.

22. The memory circuit of claim 21, wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively.

23. The memory circuit of claim 21, wherein the integrated circuit memory device is a memory device selected from the group consisting of a DRAM device, a flash memory device, a volatile memory device, a non-volatile memory device, a SRAM device, and a static memory device.

24. A memory circuit comprising:

one or more integrated circuit memory devices operable for sending and

receiving signals, wherein each of the integrated circuit memory devices operates to receive a first subset of a set of command and address signals substantially simultaneous with receiving a first edge of a first cycle of a clock signal, wherein each of the integrated memory circuit devices operates to further receive a second subset of the set of command and address signals substantially simultaneous with receiving a first edge of a second cycle of the clock signal, and wherein each integrated circuit memory device operates to perform a memory command in response to the set of received associated command and address signals received.

25. The memory circuit of claim 24wherein the second cycle is substantially subsequent to the first cycle in the clock signal.

26 The memory circuit of claim 24 wherein the first and second edges of the clock signal comprise rising and falling edges of the clock signal, respectively, wherein in the rising and falling edges comprise a transition from a logic level "zero" to a logic level "one" and a transition from the logic level "one" to the logic level "zero", respectively.

27. The memory circuit of claim 24, wherein the integrated circuit memory device is a memory device selected from the group consisting of a DRAM device, a flash memory device, a volatile memory device, a non-volatile memory device, a SRAM device, and a static memory device.

28. A system comprising:

one or more integrated circuit memory devices, wherein each of the one or more integrated circuit memory devices includes multiple data, command, and address pins; and

a bus, wherein the one or more integrated circuit memory devices are coupled via the bus to a controller through the multiple data, command, and address pins, wherein the controller operates to send command and address signals during a

clock cycle of a clock signal such that the number of command and address signals sent from the controller to the integrated circuit memory device is higher than a given number of command and address pins in each integrated circuit memory device.

29. The system of claim 28, wherein the controller is selected from the group consisting of a DRAM controller, a central processing unit (CPU), a graphics processing unit (GPU), and a processor.

30. The system of claim 28, wherein the integrated circuit memory device is a memory device selected from the group consisting of a DRAM device, a flash memory device, a volatile memory device, a non-volatile memory device, a SRAM device, and a static memory device.

31. The system of claim 28, wherein the controller is operable for sending the command and address signals during the clock cycle of the clock signal comprises sending the command and address signals upon both rising and falling edges of the clock cycle when transferring data to and from each integrated circuit memory device.

32. A semiconductor circuit comprising:

one or more integrated circuit memory devices, wherein each integrated circuit memory device comprises multiple command and address pins, wherein the command and address pins of each integrated circuit memory device are coupled to receive command and address signals, wherein the memory devices operates to receive command and address signals during a clock cycle of a clock signal such that the number of command and address signals sent to each integrated circuit memory device is higher than the multiple command and address pins available in each integrated circuit memory device.

33. The semiconductor circuit of claim 32, wherein the integrated circuit memory device is a memory device selected from the group consisting of a DRAM device, a flash memory device, a volatile memory device, a non-volatile memory device, a SRAM device, and a static memory device.

34. The semiconductor circuit of claim 32, wherein the command and address signals during the clock cycle of the clock signal is selected from the group consisting of initiating the command and address signals upon both the rising and falling edges of the clock cycle of the clock signal, initiating the command and address signals upon a rising edge of the clock cycle and further initiating address signals on a falling edge of the timing cycle, initiating the command and address signals upon two consecutive rising edges of the timing signal, and initiating the command and address signals on a rising edge of the timing cycle and further initiating the address signals on a subsequent rising edge of the timing cycle.

36. A memory circuit comprising:

one or more integrated circuit memory devices, wherein each integrated circuit memory device comprises a predetermined number of command and address pins, wherein each integrated circuit memory device is coupled to send and receive signals on the predetermined number of command and address pins, wherein the one or more memory devices operates to receive a number of command and address signals during more than one edge of a clock signal such that the number of command and address signals for each integrated circuit memory device are substantially higher than the predetermined number of command and address pins in each integrated circuit memory device.

37. The memory circuit of claim 36, wherein the integrated circuit memory device is a DRAM device.

38. The memory circuit of claim 36, wherein the command and address signals are selected from the group consisting of initiating the command and address signals upon both the rising and falling edges of the clock cycle of the clock signal, initiating the command and address signals upon a rising edge of the clock cycle and further initiating address signals on a falling edge of the timing cycle, initiating the command and address signals upon two consecutive rising edges of the timing signal, and initiating the command and address signals on a rising edge of the timing cycle and further initiating the address signals on a subsequent rising edge of the timing cycle.